**Basic Electrical Science Lab  
Course Code: EE152**

**Laboratory Manual**

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Roll No: 20CSE1030

Section: B

Academic Session: April – August 2021

**National Institute of Technology Goa**



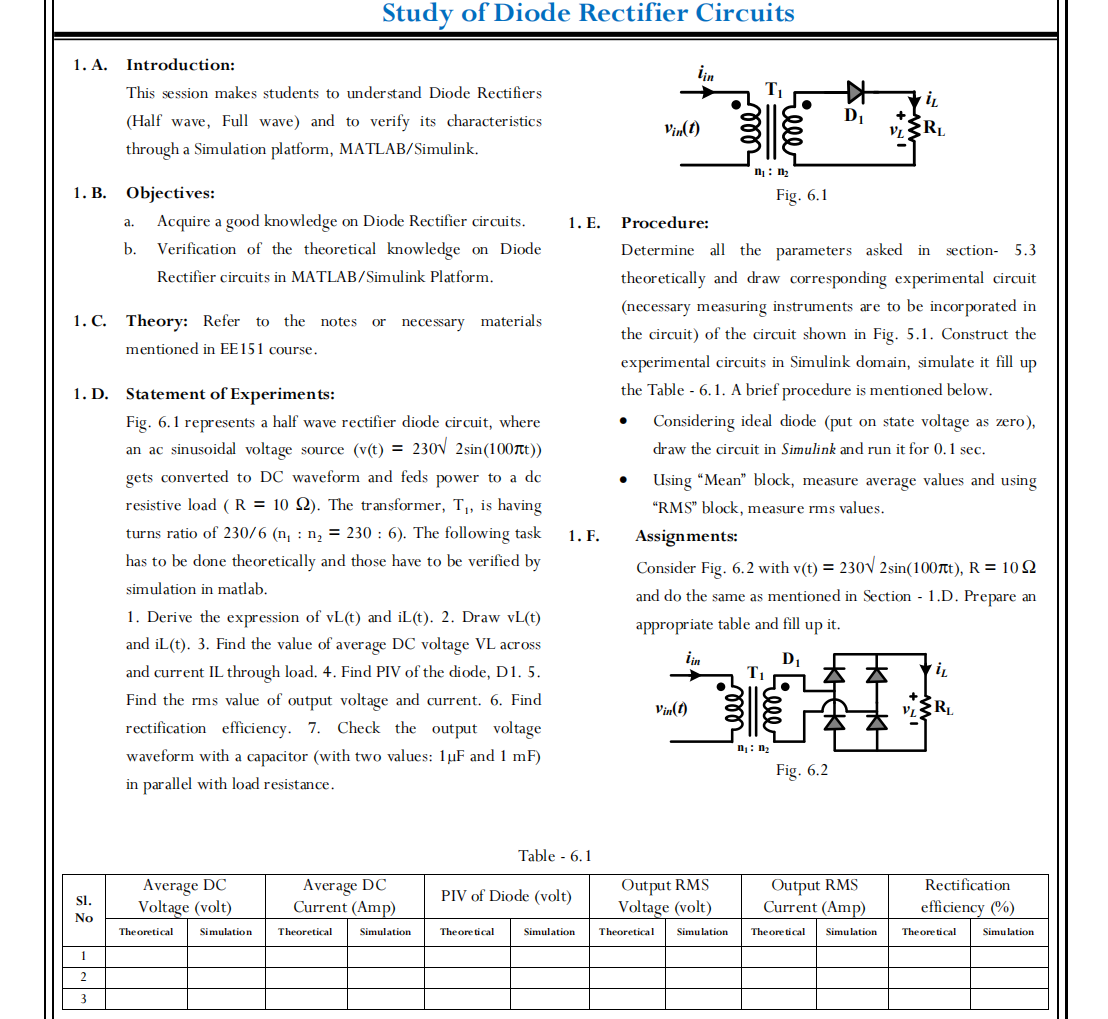
**CERTIFICATE**

This is to certify that Mr./ Ms. \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ of Class B.Tech 1st year (2nd Sem), Division Sec A/B, bearing Roll. No.\_\_\_\_\_\_\_\_\_\_\_\_\_, has satisfactorily completed the course experiments in the Laboratory Course Basic Electrical Science Lab (EE152) in the academic year 2020-2021 in the Institution of National Institute of Technology Goa.

**Course Instructor**

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| **1** | **Verification of Ohms Law** | **04** | **20-05-2021** | **23-05-2021** |  |
| **2** | **Verification of Kirchhoff's Laws – KVL and KCL** | **11** | **27-05-21** | **31-05-21** |  |
| **3** | **Verification of Thevenin’s and Norton’s Theorem** | **04** | **03-06-21** | **17-06-21** |  |
| **4** | **DC transient analysis of RC RL circuits** | **04** | **24-06-2021** | **02-07-21** |  |
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| **10** | **Digital Gate Circuits** |  |  |  |  |

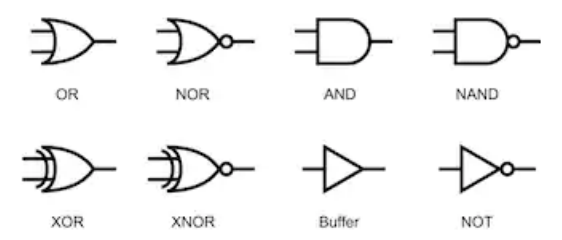
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**Experiment 5**

**Study of Diode Rectifier Circuits**

1. **Aim:** To verify the theoretical analysis of various digital combinational logic gates  
    NOT, AND, NAND, OR, NOR, XOR, XNOR
2. **Simulink Blockset used:** Diode, Linear Transformer, Resistor, Capacitor, AC voltage source, current measurement, voltage measurement, product, divide, display, scope, constant, powergui, goto, from, RMS, mean
3. **Theory:**
4. **Statement of Experiments:**

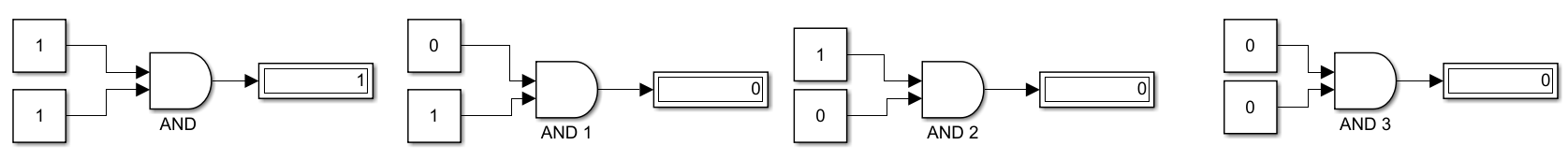
Fig. 8.1 represents various logic gates (NOT, AND, NAND, OR, NOR,XOR, XNOR). The input for these gates are digital in nature,i.e., itis either ‘0’ or ‘1’, and the output is also in digital in nature. Basedon the theoretical knowledge, a truth table for each gatehas to beprepared and that table has to be verified through simulation in Matlab/Simulink.

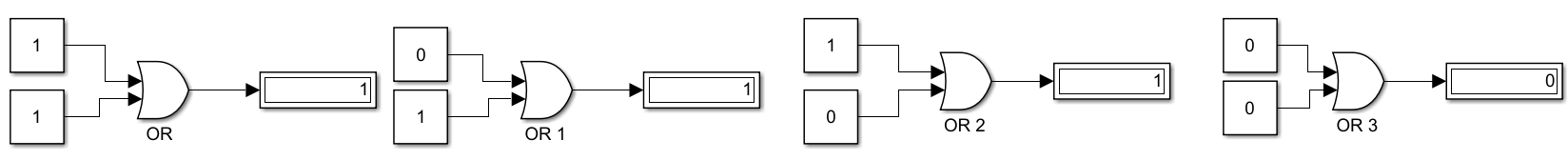


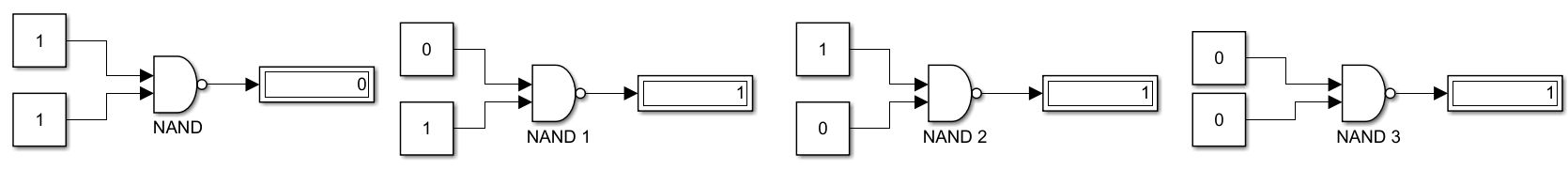
1. **Procedure:**

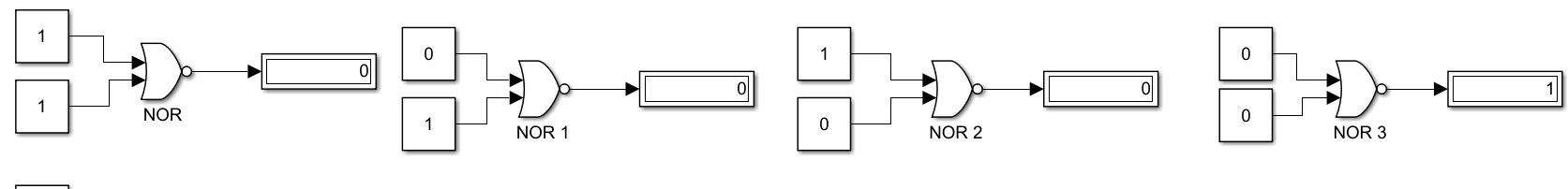
Prepare the truth table for each logic gates asked in section-8.D theoretically and draw experimental circuit (necessary Measuring instruments are to be incorporated in the circuit) corresponding to the logic gates shown in Fig. 8.1. Construct the experimental circuits in Simulink domain, simulate it, and observe the output and validate corresponding truth table against each logic gates.

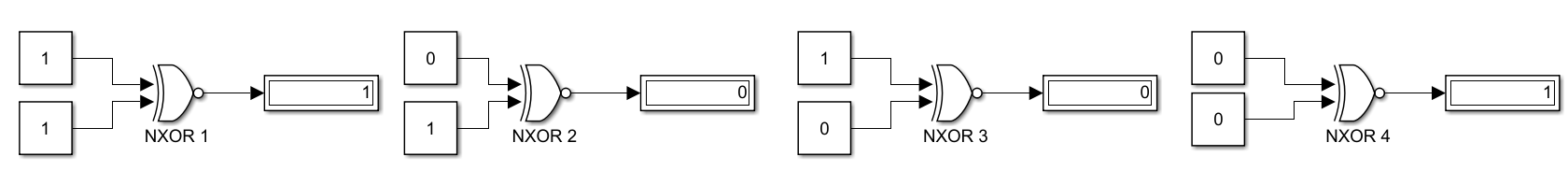
* Circuit Diagram:

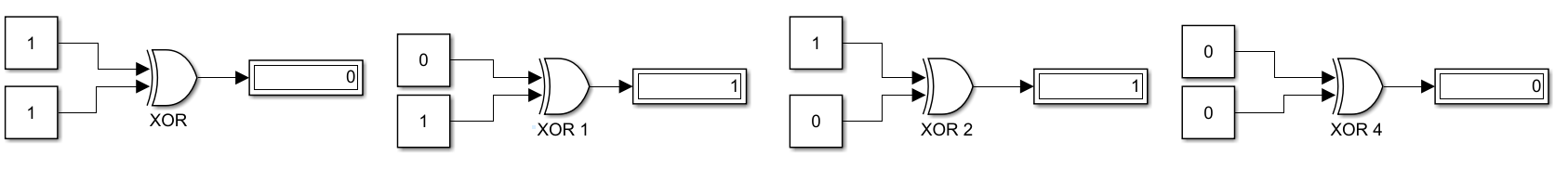


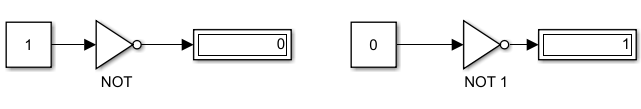












|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | SImulated |
| AND | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | SImulated |
| OR | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | SImulated |
| NAND | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 |

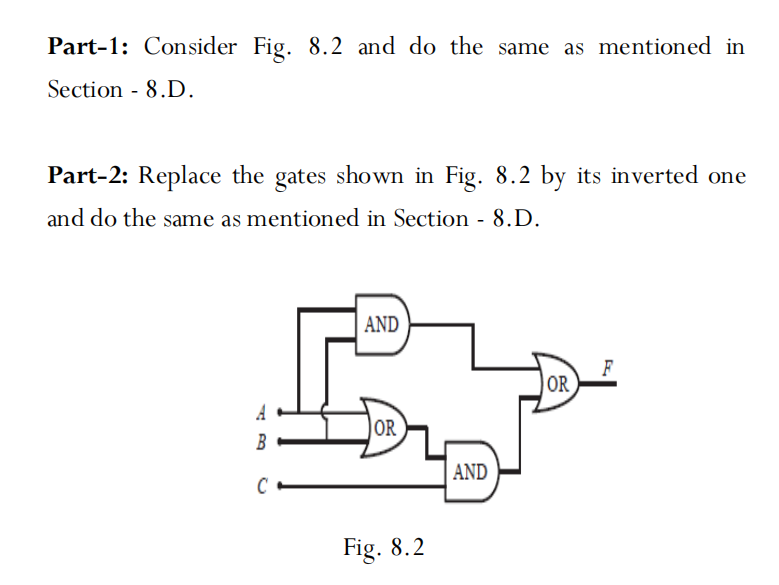
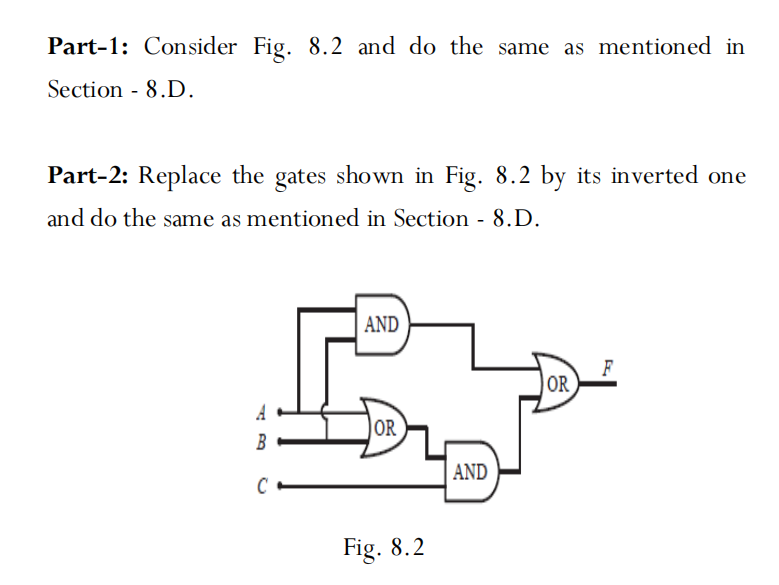
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | SImulated |
| NOR | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | SImulated |
| NXOR | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Logic Gate | Input | Input | Output | |
| Theoretical | SImulated |
| XOR | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 |

|  |  |  |  |
| --- | --- | --- | --- |
| Logic Gate | Input | Output | |
| Theoretical | SImulated |
| NOT | 1 | 0 | 0 |
| 0 | 1 | 1 |

Assignment:



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A | B | C | Output | |
| Theoretical | SImulated |
| 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 |

